

PARYLENE-STRENGTHENED THERMAL ISOLATION TECHNOLOGY FOR MICROFLUIDIC SYSTEM-ON-CHIP APPLICATIONS

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ABSTRACT

Here we reported a novel technology using parylene-cross-linking structure to achieve on-chip air-gap thermal isolation for microfluidic system-on-chip (SOC) applications. Two applications based on this technology, on-chip continuous-flow polymerase chain reaction (PCR) and on-chip temperature gradient liquid chromatography (LC) were successfully demonstrated. Device thermal performance in each example was characterized. Results showed that our technology not only provides excellent on-chip thermal isolation but also its simplicity of integration with other on-chip components makes versatile microfluidic SOC applications feasible.

Keywords: Parylene, Thermal isolation, Microfluidic, On-chip, Chromatography

INTRODUCTION

Silicon is a fundamental structure material in MEMS with a very high thermal conductivity of 148 W/m-K (compared with 73 W/m-K of iron). This specific thermal property guarantees great on-chip temperature uniformity, however it also generates design complexity for applications where multiple temperature zones are required on a single silicon chip. Some representative SOC applications that require multiple on-chip temperature zones are polymerase chain reaction [1] and temperature gradient liquid chromatography [2]. Ideally, for best temperature uniformity on each temperature zone, no silicon connection should remain between temperature zones and therefore a wafer-thickness-deep, temperature-zone-surrounding thermal isolation structure needs to be used on the chip. While several thermal isolation technologies have been developed, the aerogel or porous-silicon structure in general provides only vertical direction thermal isolation [3]; floating membrane structure which uses thin dielectric layer to hold freestanding temperature zone is mechanically fragile and cannot stand much stress and strain encountered during device fabrication or testing procedures [4]; oxide-filled trench structure has only limited thermal isolation efficiency due to the still high thermal conductivity of oxide (1.4 W/m-K for silicon dioxide) and the limited oxide thickness [5]. To attack

these shortcomings, we propose here to use a novel parylene-cross-linking thermal isolation technology.

In the past decade, parylene was used extensively as a MEMS structure material to build microfluidic system components including sensors and actuators [6-9]. Because parylene is a flexible polymer material (an elongation break of 200 %) and has a very low thermal conductivity of 0.08 W/m-K (compared with 0.03 W/m-K of static air), using parylene to build thermal isolation structure can provide crucial benefits such as robust mechanical support to the temperature zones and high thermal isolation efficiency, which in general cannot both be provided at the same time by other thermal isolation technologies. As will be shown below, we have successfully developed the parylene-strengthened thermal isolation technology and demonstrated its applications, in the field of microfluidic system-on-chip.

DESIGN AND FABRICATION

Fig. 1 shows the process flow of the proposed parylene-strengthened thermal isolation technology.

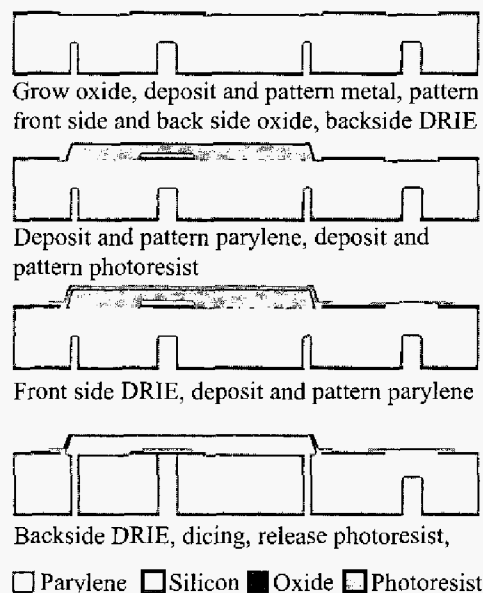


Fig. 1: Process flow of parylene-strengthened thermal isolation technology.

This technology not only provides lateral on-chip thermal isolation but also it allows microfluidic channel and electrical path connection between temperature zones. Process starts with growing 1 μm SiO_2 layer on both sides of 4-inch silicon wafers (thickness: $525 \pm 25 \mu\text{m}$) by thermal oxidation. Metal is then deposited and patterned on the wafer front side. Front side oxide is patterned with buffer HF (Transene, Danvers, MA). Backside oxide is then patterned to define the $100\mu\text{m}$ -diameter liquid access holes and $150\mu\text{m}$ -wide air gap for thermal isolation. Without removing photoresist on the backside oxide, DRIE (deep reactive ion etching) is used to etch backside silicon for $450 \mu\text{m}$. $4\mu\text{m}$ -thick parylene-C (Specialty Coating Systems, Indianapolis, IN) is then deposited and patterned with oxygen plasma on wafer front side. $25 \mu\text{m}$ photoresist AZ4620 (Clariant, Somerville, NJ) is deposited and patterned on wafer front side to form microfluidic channel sacrificial layer. A 100°C -3hr baking is carried out to avoid photoresist bubbling from latter thermal treatment. Front side oxide and photoresist are then used together as DRIE mask to etch down silicon for a $30\mu\text{m}$ -deep, $15\mu\text{m}$ -wide trenches with a mushroom profile in the trench bottom (by a modified DRIE Bosch process [10]). The trench-mushroom structure here is used as the anchoring space for parylene thin film deposition. $10 \mu\text{m}$ parylene is then conformally deposited on wafer front side, filling up the trenches and covering photoresist structures. Parylene is then patterned with oxygen plasma. DRIE is carried out on wafer backside again to etch through the silicon wafer for the liquid access holes and thermal-isolation air gaps. Finally, the wafer is diced into $1.1\text{cm} \times 1.1\text{cm}$ chips and photoresist inside the column is dissolved by 80°C -24hr acetone bath through backside liquid access holes.

Fig. 2a shows the schematic plot of parylene-cross-linking structure. Parylene layer is deposited into silicon trenches created by DRIE to provide robust parylene anchoring. Since parylene has a high elongation break and a very low thermal conductivity, parylene-cross-linking structure provides a durable

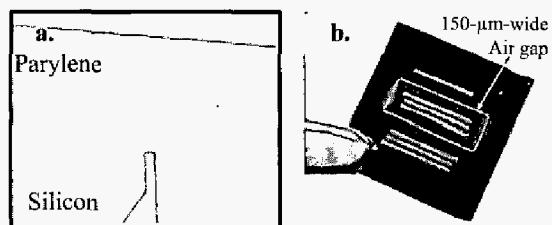


Fig. 2: a. Illustration of parylene-cross-linking structure, b. a photograph showing $150\mu\text{m}$ -wide through-wafer air gap and the silicon temperature zone (center piece).

mechanical support to temperature zones while not much heat will be conducted through the structure

itself. Fig. 2b shows a silicon temperature zone defined by $150\mu\text{m}$ -wide air gap. Fig. 3a shows the cross-sectional view of the anchored parylene column which is $100\mu\text{m}$ -wide and $25\mu\text{m}$ -high. Fig. 3b shows the fabricated microfluidic channel on top of a parylene membrane running across the thermal isolation air gap from one temperature zone to the other.

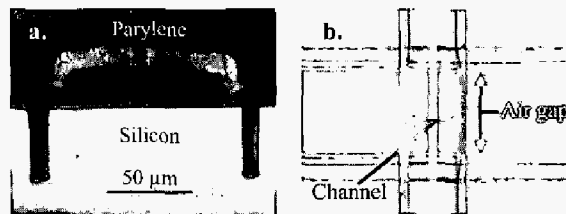


Fig. 3: a. Cross-sectional view of the anchored parylene column, b. fabricated microfluidic channel running across thermal isolation air gap.

APPLICATION AND DISCUSSION

Two examples of microfluidic SOC application using proposed parylene-strengthened thermal isolation technology were successfully carried out as follows.

On-chip continuous-flow PCR

Polymerase chain reaction requires the DNA sample solution to periodically pass through three temperature zones including the high temperature zone (94°C) for double-strand DNA (dsDNA) melting, the low temperature zone (60°C) for primer annealing and the medium temperature zone (72°C) for primer extension [1]. With the developed thermal isolation technology, three temperature zones defined by air gaps were created on the silicon substrate. Each temperature zone had its individual resistive heater for precise temperature control. As shown in Fig. 4a, 10 PCR cycles were prepared on a $0.8\text{cm} \times 0.8\text{cm}$ chip area. PCR time ratio among the three temperature zones was defined by the fluidic channel length in each temperature zone. Fig. 4b then shows the thermal image of the powered up PCR temperature zones taken by InfraScope™ system.

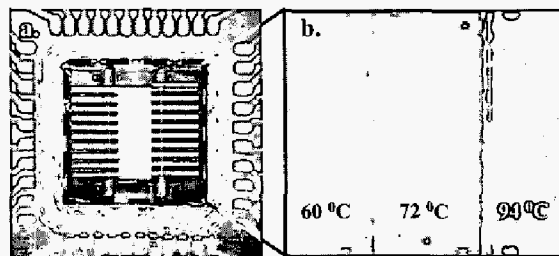


Fig. 4: a. Continuous-flow PCR device with 10 PCR cycles, b. thermal image of a powered up PCR device., temperature was read out from heater resistance via TCR (temperature coefficient of resistance) data.

On-chip temperature gradient liquid chromatography MEMS technology is a fundamental tool to carry out the miniaturization goal of modern HPLC system [11].

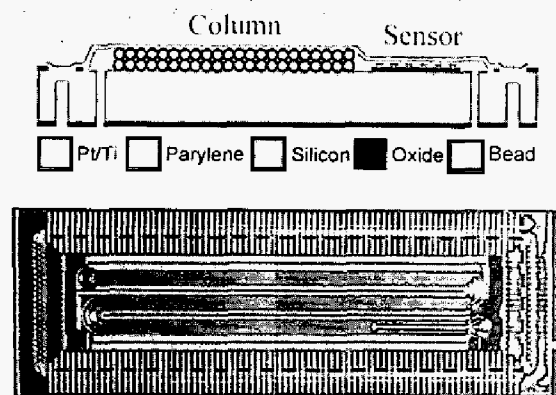


Fig. 5: On-chip temperature gradient liquid chromatography device. Dashed rectangle defines the separation column zone surrounded by 150µm-wide air gap; thin white lines are parylene cross-linking structure; running between the separation column is the resistive heater.

While most researchers have pursued solvent-controlled MEMS LC [12], temperature gradient LC (i.e., changing the LC column's temperature as a function of time to achieve analytes elution) has never been demonstrated in MEMS before [13]. In fact, we believe MEMS temperature gradient LC is extremely attractive because of the ease of achieving on-chip temperature control by MEMS [14]. Based on this motivation, we used the proposed process flow to fabricate the first chip-based temperature gradient LC system which integrated LC column, electrochemical

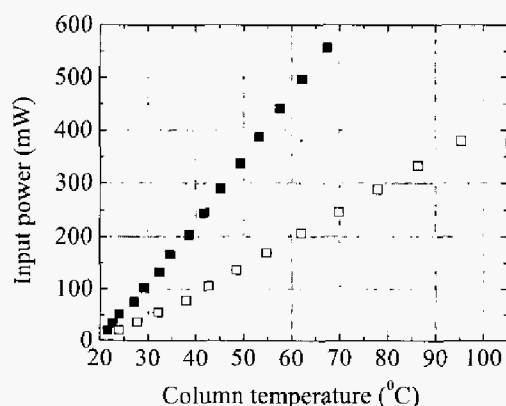


Fig. 6: Thermal isolation efficiency: (■) column without thermal isolation structure, (□) column surrounded by parylene-strengthened air-gap thermal isolation structure. Thermal isolation structure effectively reduced column-zone heating power consumption by 58%.

sensor, resistive heater and parylene-strengthened thermal isolation structure on a single silicon chip as shown in Fig. 5.

Thermal isolation efficiency of the parylene-strengthened air-gap structure was then studied. Results showed that the thermal isolation structure effectively reduced column-zone heating power consumption by 58% (Fig. 6) and the off-column temperature rise (compared with on-column temperature rise) by 67% (Fig. 7). With the off-column cooling function available, it is feasible to layout the electrochemical sensor in the cooling area when analyte sensing needs to be done at low background temperature. Chip thermal performance can be further improved by reducing the temperature-zone area or increasing the air-gap width. Fig. 8 then shows the successful separation and detection of derivatized amino acids using our chip-based temperature gradient LC system [15].

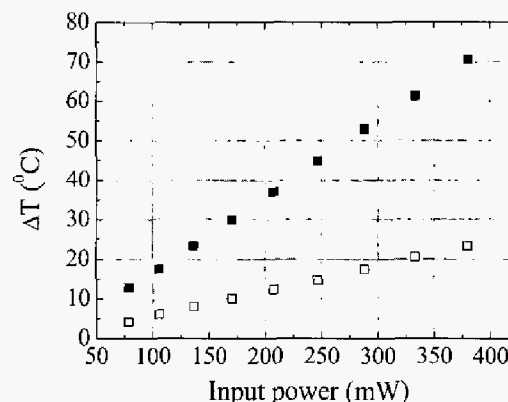


Fig. 7: On-chip temperature rise (ΔT) spatial distribution during temperature gradient operation: (■) air-gap-surrounded column area, (□) off-column area. Compared with on-column area, temperature rise in the off-column area was reduced by 67%.

CONCLUSION

A novel thermal isolation technology using parylene-cross-linking structure to achieve on-chip air gap thermal isolation was demonstrated. Two applications based on this technology, on-chip continuous-flow polymerase chain reaction and on-chip temperature gradient liquid chromatography were successfully carried out. Devices thermal performance was characterized. Results showed that our technology not only provides excellent on-chip thermal isolation efficiency but also its simplicity of integration with other on-chip components makes versatile microfluidic SOC applications feasible. Future work is focused on improving fluidic column structure robustness especially around the air gap region so to make more high pressure applications feasible.

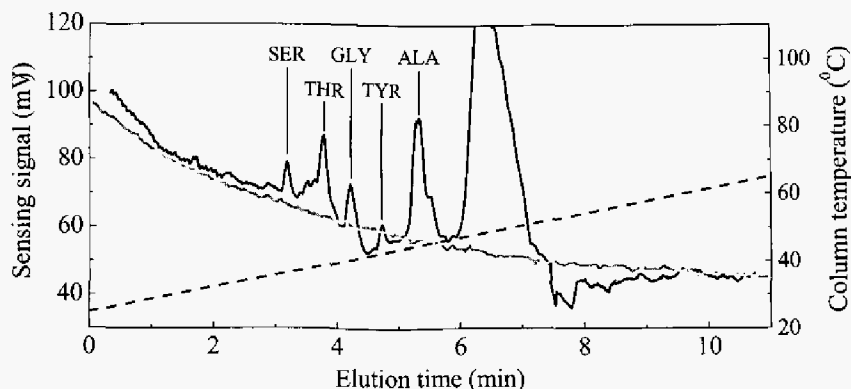


Fig. 8: Chromatogram showing derivatized amino acids separated using temperature gradient elution: (black line) temperature gradient elution with column temperature scanning from 25 °C at 0 min to 65 °C at 11 min with a slope of 3.6 °C/min, (gray line) isothermal elution with column temperature fixed at 25 °C throughout the separation, (dash line) temporal temperature gradient which was applied to the column during separation.

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